

Listing of the Claims:

Claims 1-7 (Canceled).

Claim 8 (Original): A circuit for receiving data to be written in a synchronous semiconductor memory device, comprising:

- a first set of latches for receiving an n-bit data upon transition of an internal strobe signal;
- a counter for counting the number of transitions of the internal strobe signal and for outputting an indicating signal upon counting the end of a string of internal strobe signals;
- a second set of latches for receiving the outputs of the first set of latches, the second set of latches being clocked by the indicating signal; and
- a third set of latches for receiving the outputs of the second set of latches, the third set of latches being clocked by a clock signal derived from a system clock.

Claim 9 (Original): The circuit of claim 8, wherein the counter is clocked by a first clock derived from the system clock.

Claim 10 (Original): The circuit of claim 9, wherein the first clock is derived from a falling edge of the system clock.

Claim 11 (Original): The circuit of claim 9, wherein a counter reset signal is generated based on the falling edge of the system clock after a write command, the counter reset signal for resetting the counter.

Claim 12 (Original): The circuit of claim 9, wherein the first set of latches receives the n-bit data serially under clocking control by the internal strobe signal.

Claim 13 (Original): The circuit of claim 8, wherein the second set of latches receives the latched n-bit data in parallel.

Claim 14 (Original): The circuit of claim 8, wherein the indicating signal is output by the counter upon detecting two transitions of the internal strobe signal.

Claim 15 (Original): The circuit of claim 8, wherein (n) is equal to four.

Claim 16 (Original): The circuit of claim 8, wherein the clock signal is derived by dividing by two the system clock.

Claim 17 (Original): The circuit of claim 8, wherein at least one of the first set of latches serially shifts the first and the third of the n-bit data, wherein (n) equals four.

Claim 18 (Original): The circuit of claim 8, wherein the internal strobe signal is generated from a falling edge of an external data strobe signal.

Claim 19 (Original): A circuit for receiving data to be written in a synchronous semiconductor memory device, comprising:

- a first set of latches for receiving an n-bit data upon transition of an internal strobe signal;
- a counter for counting the number of falling edges of an external strobe signal and for outputting a counting signal;

- an indicating signal generator for receiving the counting signal outputted from the counter and for outputting an indicating signal;

- a second set of latches for receiving the outputs of the first set of latches, the second set of latches being clocked by the indicating signal; and

- a third set of latches for receiving the outputs of the second set of latches, the third set of latches being clocked by a clock signal derived from a system clock.

Claim 20 (Original): The circuit of claim 19, wherein the counter is clocked by a first clock derived from the system clock.

Claim 21 (Original): The circuit of claim 20, wherein the first clock is derived from a falling edge of the system clock.

Claim 22 (Original): The circuit of claim 20, wherein a counter reset signal is generated based on the falling edge of the system clock after a write command, the counter reset signal for resetting the counter.

Claim 23 (Original): The circuit of claim 19, wherein the clock signal is derived by dividing by two the system clock.

Claim 24 (Original): A circuit for receiving data to be written in a synchronous semiconductor memory device, comprising:

- a first set of latches for receiving an n-bit data upon transition of a first internal strobe signal buffered from a data strobe buffer;

- a counter for counting the number of rising edges of a second internal strobe signal outputted from the data strobe buffer and for outputting a counting signal;

- an indicating signal generator for receiving the counting signal outputted from the counter and for outputting an indicating signal;

- a second set of latches for receiving the outputs of the first set of latches, the second set of latches being clocked by the indicating signal; and

- a third set of latches for receiving the outputs of the second set of latches, the third set of latches being clocked by a clock signal derived from a system clock.

Claim 25 (Original): The circuit of claim 24, wherein the counter is clocked by a first clock derived from the system clock.

Claim 26 (Original): The circuit of claim 25, wherein the first clock is derived from a falling edge of the system clock.

Claim 27 (Original): The circuit of claim 25, wherein a counter reset signal is generated based on the falling edge of the system clock after a write command, the counter reset signal for resetting the counter.

Claim 28 (Original): The circuit of claim 24, wherein the clock signal is derived by dividing by two the system clock.

Claims 29-40 (Canceled).